

CLAIMS

1. A method for erasing non-volatile memory cells in an integrated non-volatile memory device that comprises a memory cell array organized in a row-and-column layout, and divided in array sectors, the method comprising:
 - forcing an incompletely erased sector into a read condition;
 - scanning the rows of said sector to check the possible presence of a spurious current indicating a fail state;
 - identifying and electrically isolating the failed row;
 - re-addressing from said failed row to a redundant row within a threshold distance of the failed row; and
 - re-starting the erase algorithm.
2. A method according to claim 1, characterized in that said reading condition is forced whenever the issue of the erase algorithm is incomplete or negative.
3. A method according to claim 1, characterized in that the rows of a given sector are scanned, also checking the possible presence of said spurious discharge current in a conduction path leading to a positive power.
4. A method according to claim 1, characterized in that at least one switch is provided between each one of the decode blocks and respective positive and negative power supplies in order to isolate the failed row.
5. A method according to claim 1, characterized in that said re-addressing is effected by means of a redundancy decode block incorporated inside the row decode circuitry.

6. A method according to claim 4, characterized in that said switches are driven by a logic operatively interlinked to the contents of redundancy registers.

7. A method according to claim 3, characterized in that said spurious current is detected by comparison of a row node with a redundancy node.

8. A method according to claim 7, characterized in that said comparison is effected by a compare block, that is input a reference signal produced from a redundant row and a row signal taken at the beginning of a row being scanned.

9. The method according to claim 1 wherein the redundant row is adjacent the same sector as the sector containing the failed row.

10. The method according to claim 1 wherein the redundant row is in the same sector as the sector containing the failed row.

11. An integrated non-volatile memory device of the programmable and electrically erasable type, comprising a memory cell array organized in a row-and-column layout, and divided in array sectors, each including at least one row decode circuit portion being supplied positive and negative voltages, characterized in that it comprises:

a redundant row block inside each sector;

a plurality of row decode blocks and at least one redundancy decode block within the decode circuitry; and

at least one switch between each one of the decode blocks and the respective positive and negative supplies in order to isolate a failed block during read, program or erase operations.

10. A device according to claim 9, characterized in that said switches are MOS transistors.

11. A device according to claim 9, characterized in that it includes a control logic for controlling said switches.

12. A device according to claim 9, characterized in that the operation of said logic is interlinked with the contents of redundancy registers.

13. A device according to claim 9, characterized in that it includes a comparing block, and that said comparing block is input a reference signal produced by a redundant row and a row signal taken at the start of a row being scanned.